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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/804,146	03/19/2004	Yu Pen Tsai	4459-141	6402

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EXAMINER	
ARORA, AJAY	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 08/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/804,146	TSAI ET AL.	
	Examiner	Art Unit	
	Ajay K. Arora	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *6/8/06*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 11 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 11 recites "the positioning step and the printing step are performed synchronously". However, the positioning step must precede the printing step in order for the printing mechanism to determine where to print.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 2, 3,12 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Peterson (US 2003/0157762), hereinafter Peterson.

Regarding Claim 2, Peterson discloses a method of marking wafer-level chip scale packages, the method comprising the steps of:

providing a wafer (100) having a plurality of dice (110) formed thereon, wherein the dice have been packaged into a plurality of semi-finished chip scale packages, wherein each of the semi-finished chip scale packages comprises a plurality (page 3, para 0031, 5th sentence) of terminals (114) for making external electrical connections (page 3, para 0031, last sentence), each die has a plurality of bonding pads on an active surface thereof, the bonding pads are electrically connected to the respective terminals (page 3, para 0031, last sentence), and a backside surface of each die is exposed from a surface of the respective semi-finished chip scale package;

positioning the semi-finished chip scale packages formed on the wafer; printing ink marks by transferring ink (page 4, para 0035, last line) from a printing device onto the exposed backside surfaces of the dice (page 3, para 0032, 1st sentence);

curing the ink marks on the dice (page 4, para 0038, 2nd sentence); and

dicing the wafer (page 3, 0033, last sentence) to obtain a plurality of separated chip scale packages.

Regarding Claim 3, Peterson teaches the method further comprising the step of removing defective ink marks after the printing step and before the curing step (page 4, para 0038, 4th sentence).

Regarding Claim 12, Peterson teaches the printing step comprises the step of applying ink (page 4, para 0035, last line) in a recognizable (page 5, para 0042, 2nd last sentence) pattern directly on the exposed backside surface of the dice to form said ink marks.

Regarding Claim 13, Peterson teaches that the printing step comprising the step of applying ink (page 4, para 0035, last sentence) in a recognizable (page 5, para 0042, 2nd last sentence) pattern indicative of an identifier of each said die directly (page 3, para 0034, 2nd sentence and page 4, para 0035, last sentence) on the exposed backside surface of the die.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Peterson in view of Kim (US 6,187,615), hereinafter Kim.

Regarding claim 1, Figures 1 and 2 of Peterson disclose a chip scale package comprising: a chip (110) having a plurality of bonding pads on an active surface thereof

(page 3, para 0031, 2nd last sentence), wherein a backside surface of the chip is exposed from a surface of the chip scale package;
a plurality of terminals (114) for making external electrical connections (page 3, para 0031, last sentence), the terminals electrically connected to the bonding pads; and
an ink mark formed on the backside surface (page 3, para 0032, 1st sentence) of the chip.

However, Peterson fails to teach that a redistribution layer is disposed on the active surface of the chip and the plurality of terminals are disposed on the redistribution layer. Kim teaches (refer to Figure 14) a redistribution layer (17) disposed on the active surface of a chip (with pad 12) wherein terminals (32) are disposed on the redistribution layer. It would have been obvious to one of ordinary skills in the art at the time of the invention to modify Peterson so that a redistribution layer is disposed on the active surface of the chip and a plurality of terminals are disposed on the redistribution layer. The ordinary artisan would have been motivated to modify Peterson at least for the purpose of to provide a location of terminals that correspond to printed circuit board layout (Col. 4, lines 17-21).

Note that Peterson discloses packaged devices (page 3, para 0030, 1st sentence), which includes chip scale packages (page 1, para 0004). Further note that Peterson cites that the mark is formed with a marking medium 10 comprising underlying contrast

film 132 and the outer contrast film 134 marking medium (page 5, para 0042, 2nd sentence), wherein 132 and 134 can be inks (page 4, para 0035, last sentence).

Regarding claims 7 and 8, Figure 1 and 2 of Peterson teaches a semiconductor wafer (100) comprising a plurality of dice (110) wherein each of said dice has a plurality of bonding pads (array 114) on an active surface thereof,
a plurality of terminals (114) for making external electrical connections (page 3, para 0031, last sentence), the terminals electrically connected to the bonding pads; and
an ink mark (132 and 134) on a backside surface thereof.

However, Peterson fails to teach that a redistribution layer is disposed on the active surface of the chip and the plurality of terminals are disposed on the redistribution layer. Kim teaches (refer to Figure 14) a redistribution layer (17) disposed on the active surface of a chip (with pad 12) wherein terminals (32) are disposed on the redistribution layer. It would have been obvious to one of ordinary skills in the art at the time of the invention to modify Peterson so that a redistribution layer is disposed on the active surface of the chip and a plurality of terminals are disposed on the redistribution layer. The ordinary artisan would have been motivated to modify Peterson at least for the purpose of to provide a location of terminals that correspond to printed circuit board layout (Col. 4, lines 17-21).

Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Peterson in view of Schramm (US 2004/0060910), hereinafter Schramm.

Regarding Claim 4 and 6, Peterson teaches the method as claimed in claim 2, wherein the positioning step is performed by a positioning device (page 1, para 0005, 2nd last sentence) and further teaches a printing device (page 6, para 0049, 3rd line). However, Peterson does not teach that "the positioning device and the printing device are positioned on two opposing sides of the wafer, and the printing step is performed by coaxially aligning the printing device with the positioning device".

Figure 2c of Schramm teaches a system for marking semiconductor wafers wherein the positioning device (142) and the printing device (147) are positioned on two opposing sides of the wafer (143), and the printing step is performed by coaxially aligning (along 149) the printing device with the positioning device. It would have been obvious to one of ordinary skills in the art at the time of the invention to modify the invention of Peterson with the teachings of Schramm so that the positioning device and the printing device are positioned on two opposing sides of the wafer, and the printing step is performed by coaxially aligning the printing device with the positioning device. The ordinary artisan would have been motivated to modify Peterson for at least the purpose of improving positional accuracy.

Regarding Claim 5, Figure 2 of Peterson (page 3, para 0033, last line) teaches the wafer has a plurality of dicing streets (117) between the semi-finished chip scale packages. However, Peterson fails to teach that "the positioning step is performed by finding the dicing street with a charge coupled device (CCD)". Schramm discloses a system for processing semiconductor wafers wherein the position step is performed by finding the dicing street (page 5, para 0078, 10th sentence) with a charge coupled device (page 5, para 0076, 1st line). It would have been obvious to one of ordinary skills in the art at the time of the invention to modify the invention of Peterson with the teachings of Schramm so that the position step is performed by finding the dicing street with a charge coupled device (CCD). The ordinary artisan would have been motivated to modify Peterson for at least the purpose of utilizing widely available off-the-shelf positioning equipment.

Claims 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Peterson in view of Grigg (US 6,703,105), hereinafter Grigg.

Regarding claim 9, Peterson teaches substantially the claimed method, including that the printing step is performed by marking the backside surfaces of the dice, but does not teach that the step is performed for "all of the dice in one action". Grigg teaches a marking method for semiconductor chips, wherein the marking step may be performed for all of the dice in one action (Col. 7, lines 38-41). It would have been obvious to one of ordinary skills in the art at the time of the invention to modify the invention of

Peterson so that the printing step is performed for all of the dice in one action. The ordinary artisan would have been motivated to modify Peterson for at least the purpose of shortening the cycle time for individual chips.

Regarding claim 10, Peterson teaches substantially the claimed method, including the semi-finished chip scale packages, but does not teach that they are "positioned simultaneously". Grigg teaches a marking method for semiconductor chips/packages, wherein the chips/packages are positioned simultaneously (Col. 12, lines 47-50 and Col. 7, lines 38-41). It would have been obvious to one of ordinary skills in the art at the time of the invention to modify the invention of Peterson so that the chip scale packages are positioned simultaneously. The ordinary artisan would have been motivated to modify Peterson for at least the purpose simultaneous printing for shortening the cycle time for individual chips.

Regarding claim 11, in as much as understood, Peterson teaches substantially the claimed method but does not teach that the positioning step and the printing step are performed synchronously. Grigg teaches a marking method for semiconductor chips/packages, wherein the positioning step and the printing step are performed synchronously (Col. 12, lines 47-50, Col. 7, lines 38-41, and Col. 13, lines 34-37)). It would have been obvious to one of ordinary skills in the art at the time of the invention to modify the invention of Peterson so that the positioning step and the printing step

are performed synchronously. The ordinary artisan would have been motivated to modify Peterson for at least the purpose reducing the cycle time for printing.

Response to Arguments

Applicant's arguments with respect to claims 1, 7, 8 and 9-13 have been considered but are moot in view of the new ground(s) of rejection.

Regarding claim 2, candidate argues on pages 6 and 7 that the forming of the mark in Peterson is performed by "exposing the marking medium 120 to light", whereas in amended claim 2, it is performed by "transferring ink from printing device onto the backside surface of the die". This argument is not persuasive. Whereas Peterson does describe exposing the marking medium to light in one of the embodiments, it does not change the fact that Peterson also teaches that the marking medium can be ink (page 4, para 0035, last line). Further, any device used to apply the ink would qualify as a "printing device". Therefore, Peterson teaches transferring ink from printing device onto the backside surface of the die.

In response to applicant's argument regarding claims 4-6 on pages 8-9 that Schramm's "laser-based marking method" is nonanalogous art, it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned,

in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, both the claimed invention and the Schramm reference teach marking systems for semiconductor dies and wafers.

Conclusion

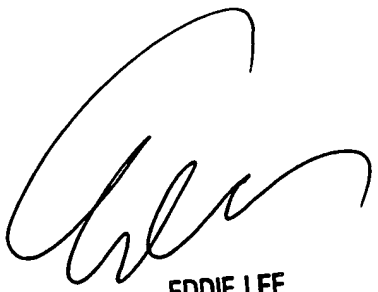
Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ajay K. Arora whose telephone number is (571) 272-8347. The examiner can normally be reached on Mon through Fri, 8am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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